IN THE SPECIFICATION

Please amend below paragraph of the specification as follows:

[1151] As illustrated in FIG. 14, information bits $I[0]:I[3]$ are presented to an encoder 1200, similar to encoders 1500 and 1100. The encoder 1100 includes a look ahead state generator 1200 for applying Equations (16) and (17) to the input information bits $I[0]:I[3]$. The look ahead state generator 1202 generates the state information and stores the states $S0[4]$, $S1[4]$, $S2[4]$ in a register or memory storage device 1204. The state information is updated on each system clock cycle. Prior to storing the first values, ~~stored in~~ the memory storage device 1204 is initialized to predetermined state values. The state values $S0[0]:S0[3]$, $S1[0]:S1[3]$, $S2[0]:S2[3]$ are then provided to multi-bit output generators 1206, 1208. The input information bits $I[0]:I[3]$ are provided as the outputs $X[0]:X[3]$. The multi-bit output generator 1206 generates the outputs $Y_0[0]:Y_0[3]$; while the multi-bit output generator 1208 generates the outputs $Y_1[0]:Y_1[3]$. The multi-bit output generators 1206 and 1208 recursively calculate values based on Equations (16) and (17) given hereinabove.